Optimization of Surface Planarization of Si/SiGe Virtual Substrates for Use in Quantum Computational Devices

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The creation of highly coherent qubits is crucial to the realization of large-scale quantum computers, which have been proven theoretically to significantly speed up the solution of difficult problems in computing.1,2 This project aims to contribute to ongoing efforts in fabricating gate-confined, single-electron spin qubits in a strained, isotopically enriched3 Si/SiGe heterostructure.4 To strain the Si layer and enhance electron confinement, the device structure contains a graded buffer of Si and Ge referred to as the virtual substrate (VS). However, due to the relaxation of the lattice after VS growth, a crosshatch pattern develops at the surface of the virtual substrate. The surface roughness caused by the crosshatch pattern presumably traps additional electrons, which decrease the coherence time of the qubit spin state. In order to increase the likelihood of successful qubit formation, we employ a process called chemical mechanical planarization (CMP) to obtain an atomically flat surface in the VS plane. To characterize the roughness of the material surface before and after CMP, we use atomic force microscopy and laser scanning microscopy, which we also use to measure change in material thickness. Excessive removal of material during CMP can lead to a breakdown of the VS structure, which causes device failure. Consequently, we aim to determine the optimal parameters for achieving an atomically flat surface at the VS/Si interface while removing as little material possible from the VS to fabricate viable spin qubits.

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Motivation

Quantum Computing
- Speeds up key problems in computing1,2
- Motivates development of a new field of algorithms research
- Brings us closer to the physical limits of computation

Bits and Qubits
Classically, information can only be in 2 states: 0 or 1. In quantum, a qubit can be in a superposition of the |0⟩ and |1⟩ states

Advantages of Qubits
- Parallel computation
- Higher information density

Fabrication & Background

Qubit Representation
- Single-electron spin qubit device.
- Information encoded using phase and magnitude of spin precession

Single-electron Confining Device
- Electrically controllable4
- Scalable

Si/SiGe Heterostructure
- Maintains spin coherence3
- Traps electrons at interface between Si and SiGe

Challenges
- Formation of crosshatch pattern
- Additional trapping of electrons

Goal
- Minimize the impact of polishing on material structure

Experimental Methods

Chemical Mechanical Planarization (CMP)
Softens and/or etches the material surface chemically
Uses friction to remove particles at the surface.

Chemical Cleaning6
Removes colloidal silica particles
Prevents surface contamination

Measurement
1. Laser Microscopy
Records changes in thickness between sample and reference wafers

2. Atomic-force Microscopy (AFM)
Characterizes surface roughness during final stages of polishing

Results

Before CMP
Laser Microscope at 150x

After CMP
Laser Microscope at 10x

Discussion

- KOH used instead of NH4OH in the polishing slurry
  - Si was etched anisotropically
  - Slight macroscopic roughness remained
  - Substrate edges were polished faster than the surface center
- Si used instead of SiGe to practice technique at low cost
- Limited available expertise on CMP

Conclusions
- Eliminated local surface roughness on Si
- Developed the foundations of CMP procedure for the laboratory

Future Work
- Overhaul CMP machinery and improve experimental setup
- Characterize the polishing rate of SiGe under set pressure, velocity, and slurry conditions
- Finalize the procedure for CMP to be used in device fabrication

References


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