

# Optimization of Surface Planarization of Si/SiGe Virtual Substrates for Use in Quantum Computational Devices

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The creation of highly coherent qubits is crucial to the realization of large-scale quantum computers, which have been proven theoretically to significantly speed up the solution of difficult problems in computing.<sup>1,2</sup> This project aims to contribute to ongoing efforts in fabricating gate-confined, single-electron spin qubits in a strained, isotopically enriched<sup>3</sup> Si/SiGe heterostructure.<sup>4</sup> To strain the Si layer and enhance electron confinement, the device structure contains a graded buffer of Si and Ge referred to as the virtual substrate (VS). However, due to the relaxation of the lattice after VS growth, a crosshatch pattern develops at the surface of the virtual substrate. The surface roughness caused by the crosshatch pattern presumably traps additional electrons, which decrease the coherence time of the qubit spin state. In order to increase the likelihood of successful qubit formation, we employ a process called chemical mechanical planarization (CMP) to obtain an atomically flat surface in the VS plane. To characterize the roughness of the material surface before and after CMP, we use atomic force microscopy and laser scanning microscopy, which we also use to measure change in material thickness. Excessive removal of material during CMP can lead to a breakdown of the VS structure, which causes device failure. Consequently, we aim to determine the optimal parameters for achieving an atomically flat surface at the VS/Si interface while removing as little material possible from the VS to fabricate viable spin qubits.

<sup>1</sup>P. Shor, *SIAM Journal of Computing* **26**, 1484-1509 (1997).

<sup>2</sup>W. L. Chang, *Emerging Research in Artificial Intelligence and Computational Intelligence: Int. Conf. Proc.* **237**, 483-490 (2011).

<sup>3</sup>K. M. Itoh and H. Watanabe, *MRS Communications* **4**, 143-157 (2014).

<sup>4</sup>E. Kawakami, *et al.*, *Nature Nanotech.* **9**, 666-670 (2014).



# Optimizing the Surface Planarization of Si/SiGe Virtual Substrates for Applications in Quantum Computing



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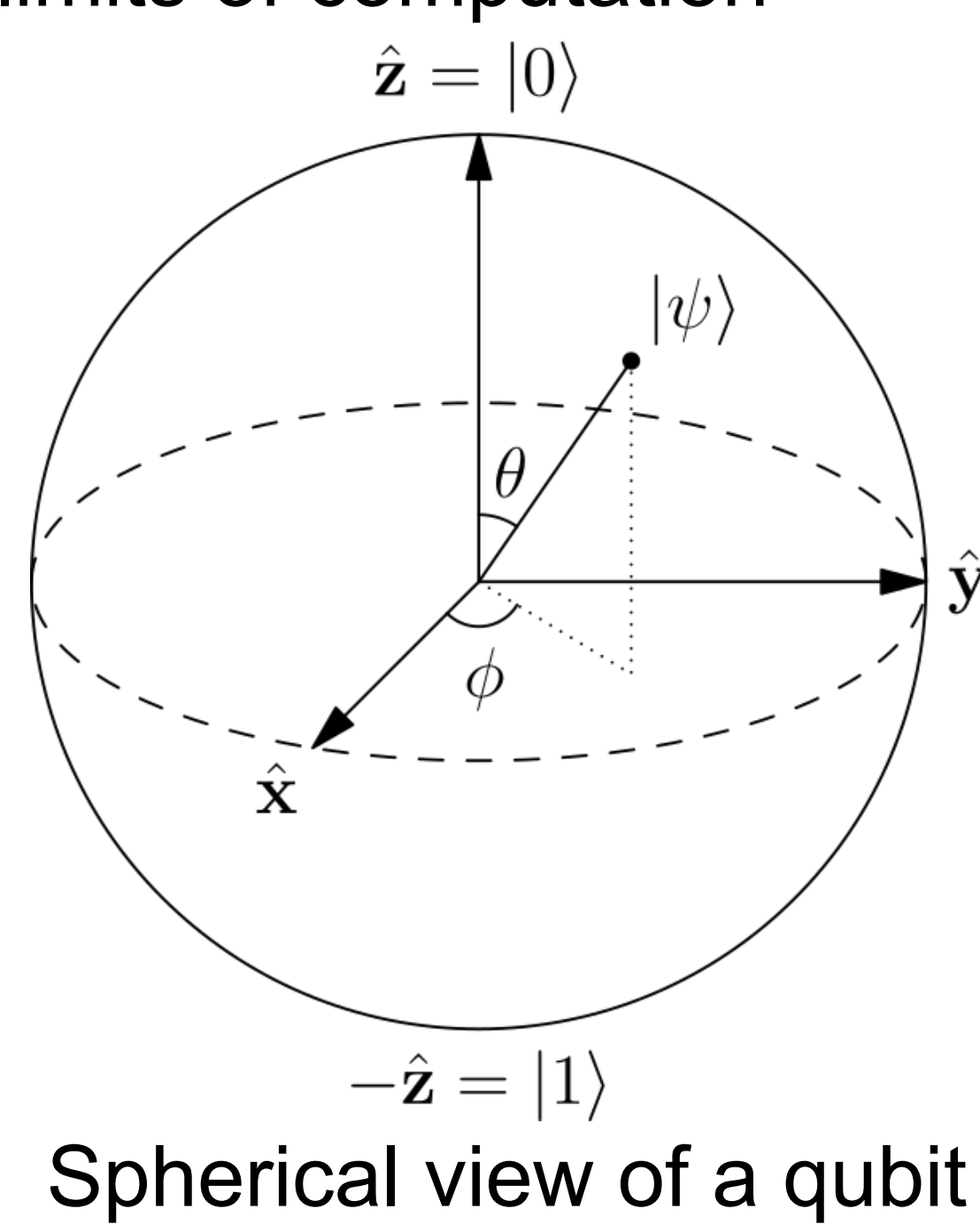
## Motivation

### Quantum Computing

- Speeds up key problems in computing<sup>1,2</sup>
- Motivates development of a new field of algorithms research
- Brings us closer to the physical limits of computation

### Bits and Qubits

Classically, information can only be in 2 states: 1, or 0. In quantum, a qubit can be in a superposition of the  $|0\rangle$  and  $|1\rangle$  states



### Advantages of Qubits

- Parallel computation
- Higher information density

## Fabrication & Background

### Qubit Representation

- Single-electron spin qubit device.
- Information encoded using phase and magnitude of spin precession

### Single-electron Confining Device

- Electrically controllable<sup>4</sup>
- Scalable

### Si/SiGe Heterostructure

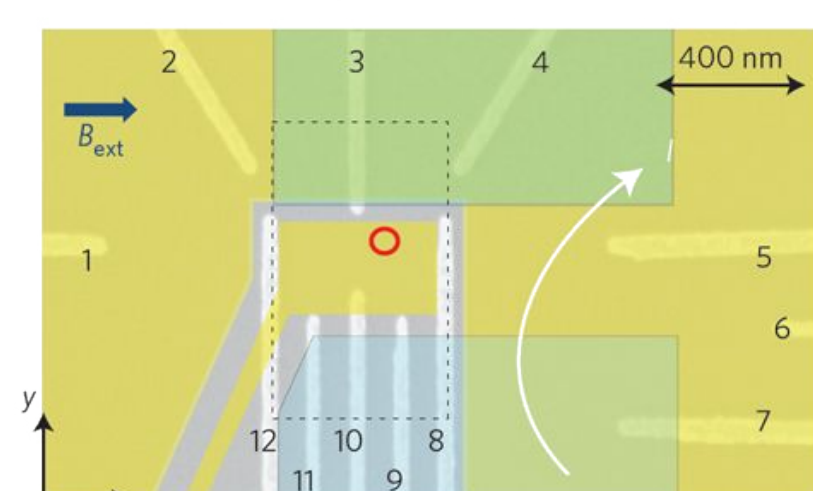
- Maintains spin coherence<sup>3</sup>
- Traps electrons at interface between Si and SiGe

### Challenges

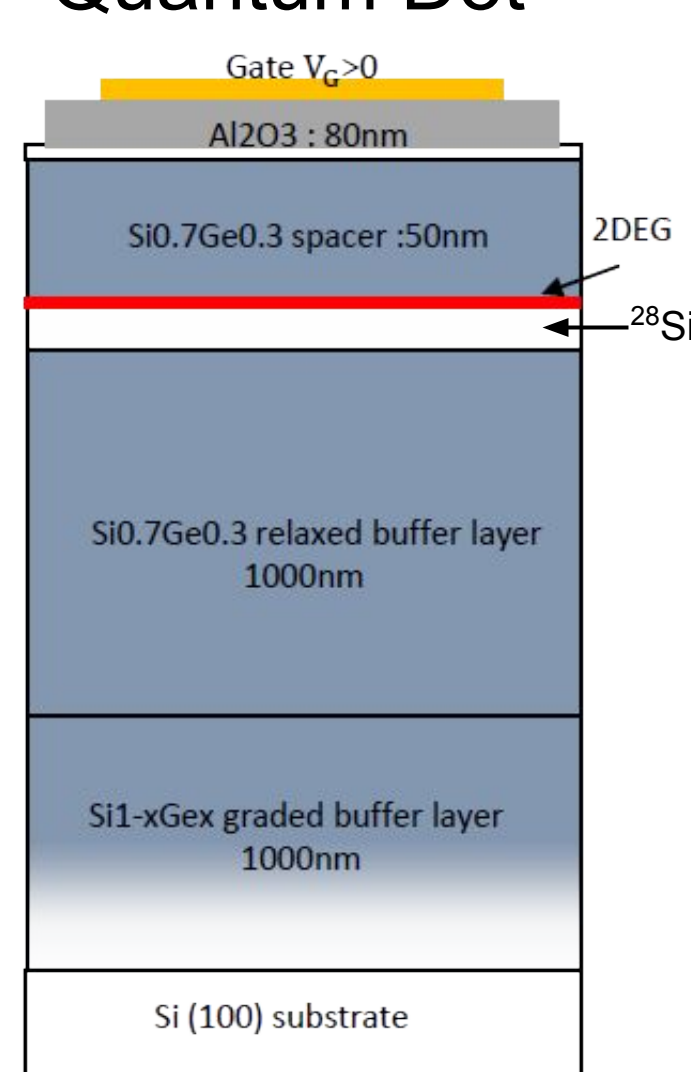
- Formation of crosshatch pattern
- Additional trapping of electrons

### Goal

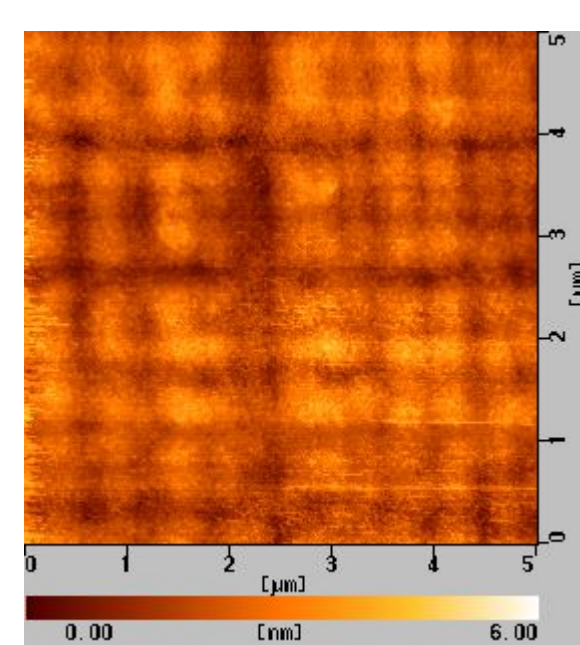
- Minimize the impact of polishing on material structure



Gate-confined Quantum Dot<sup>4</sup>



Example Si/SiGe Heterostructure<sup>5</sup>



Crosshatch Pattern

## Experimental Methods

### Chemical Mechanical Planarization (CMP)

Softens and/or etches the material surface chemically  
Uses friction to remove particles at the surface.

### Chemical Cleaning<sup>6</sup>

Removes colloidal silica particles  
Prevents surface contamination

### Measurement

#### 1. Laser Microscopy

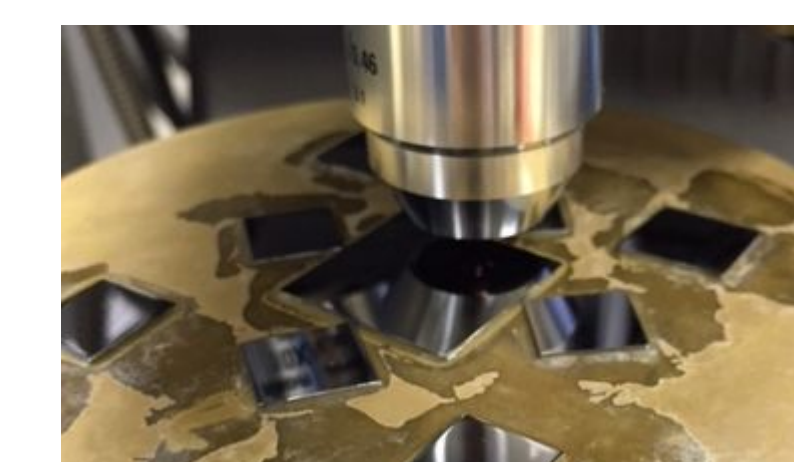
Records changes in thickness between sample and reference wafers

#### 2. Atomic-force Microscopy (AFM)

Characterizes surface roughness during final stages of polishing



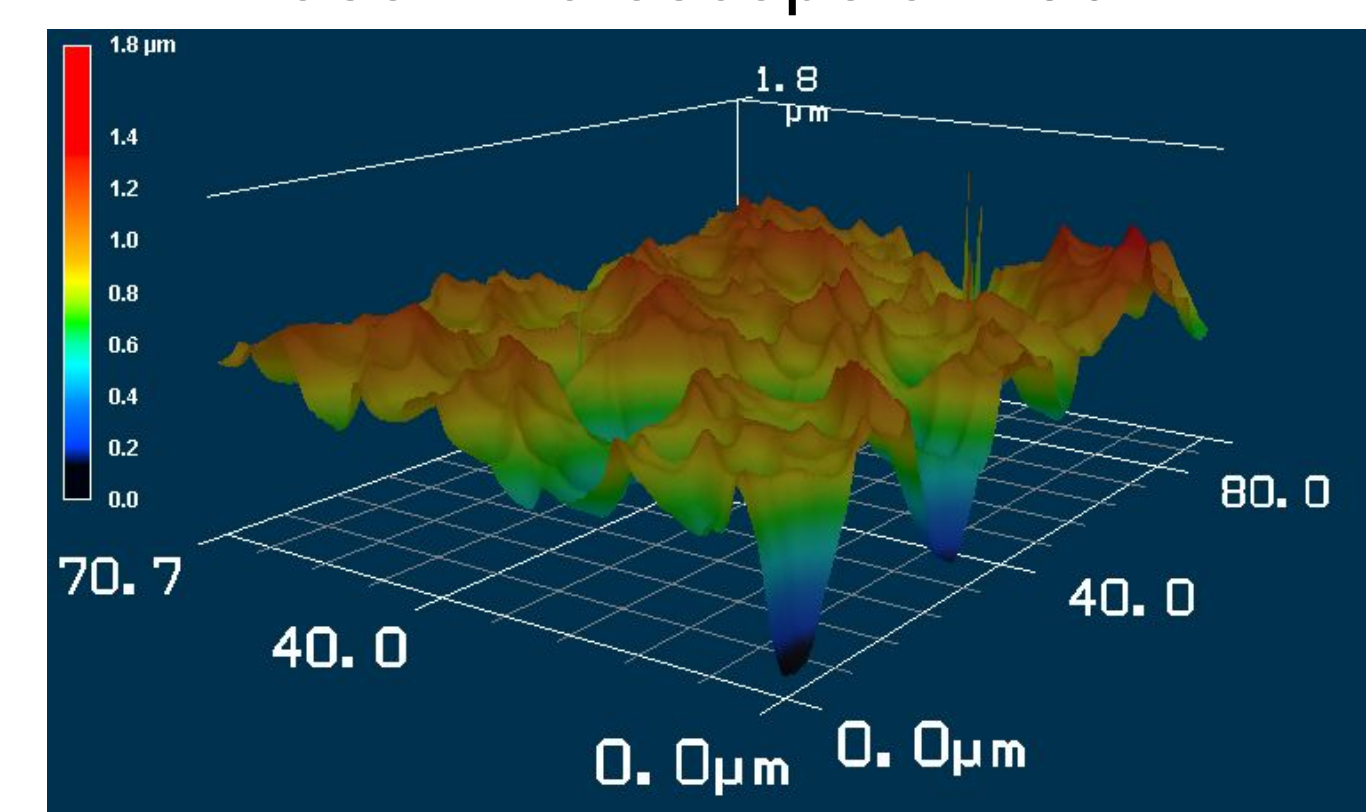
Lapping machine during CMP



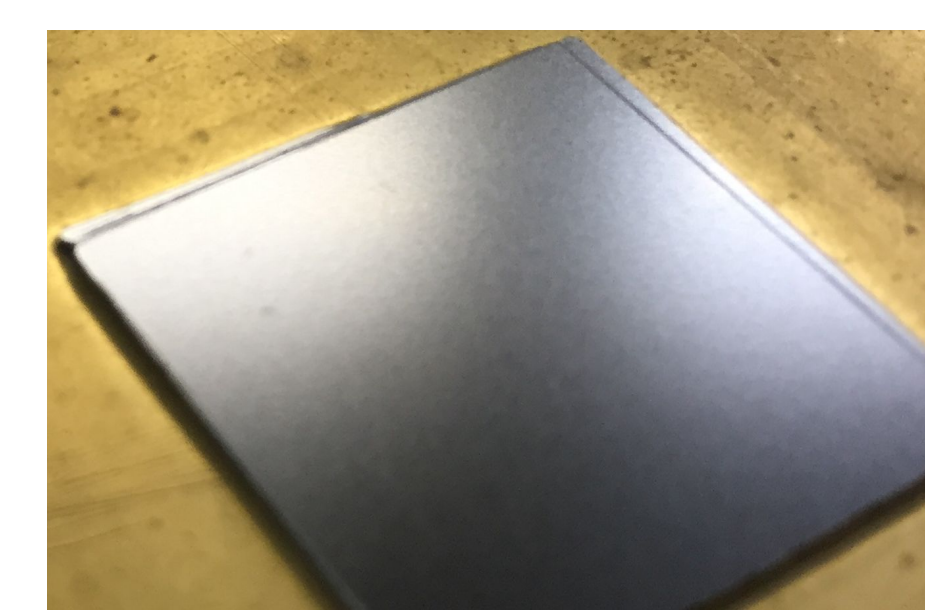
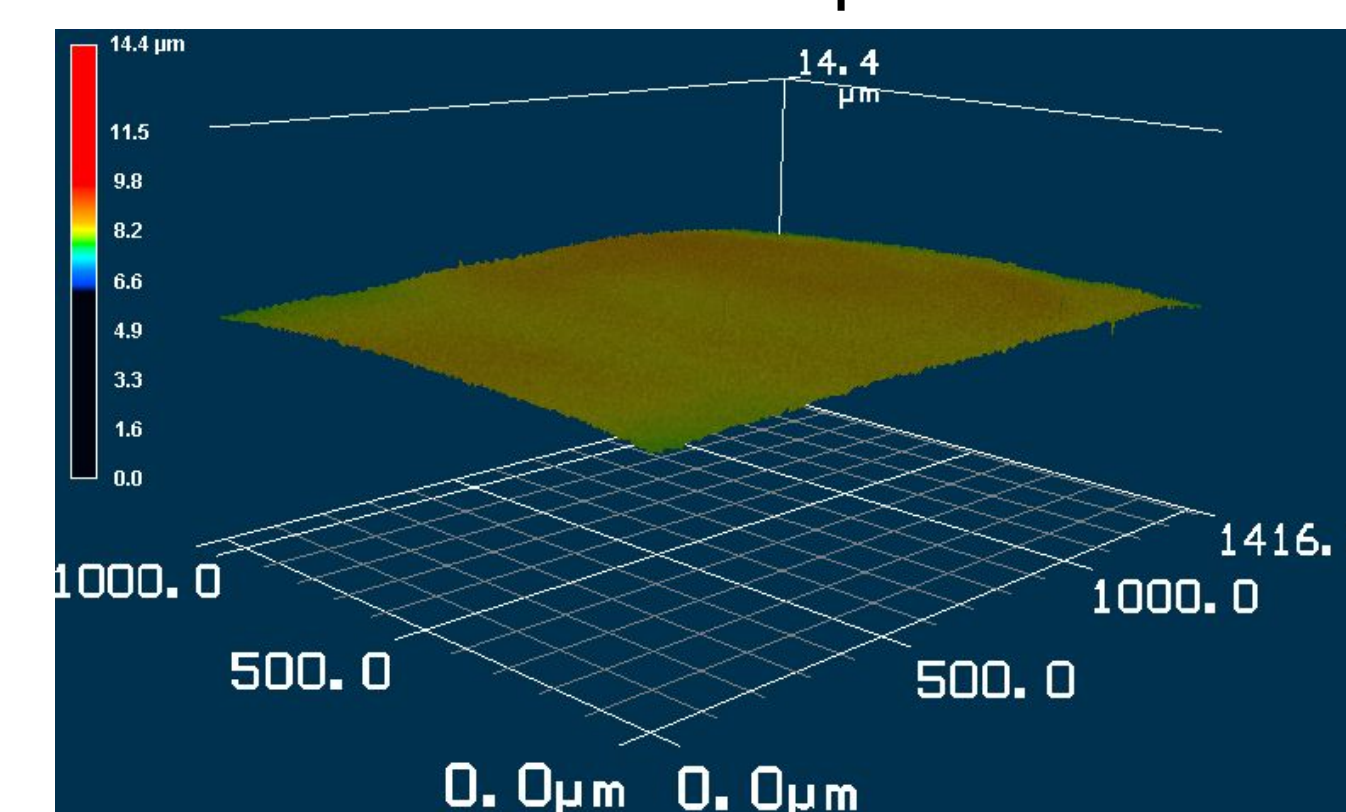
Measuring thickness change

## Results

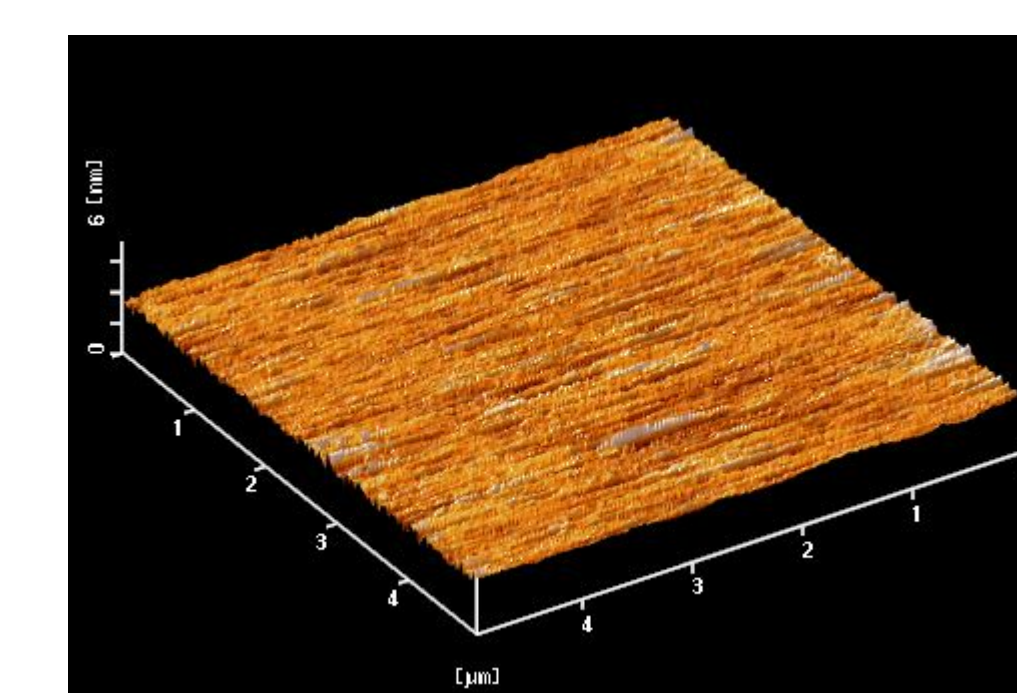
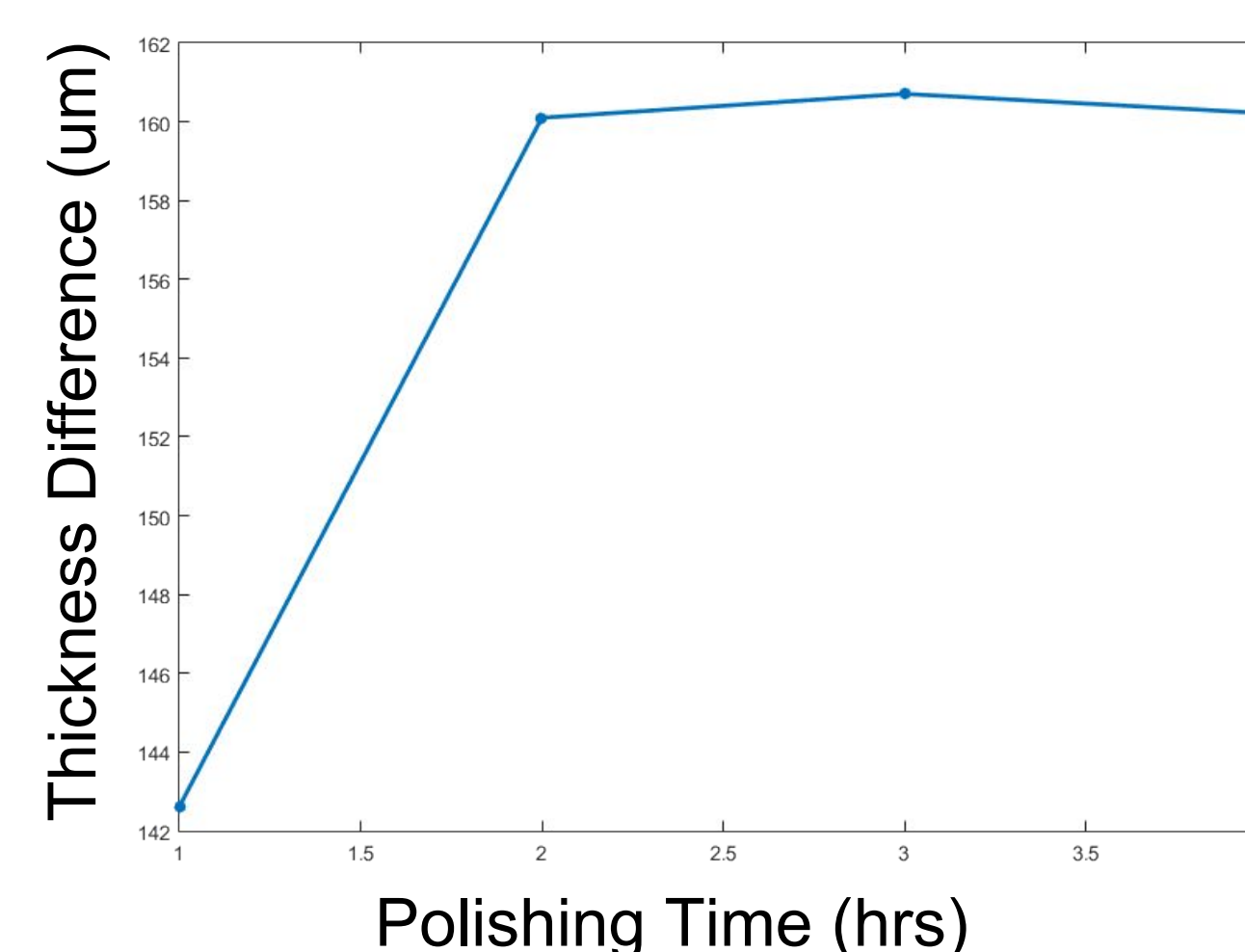
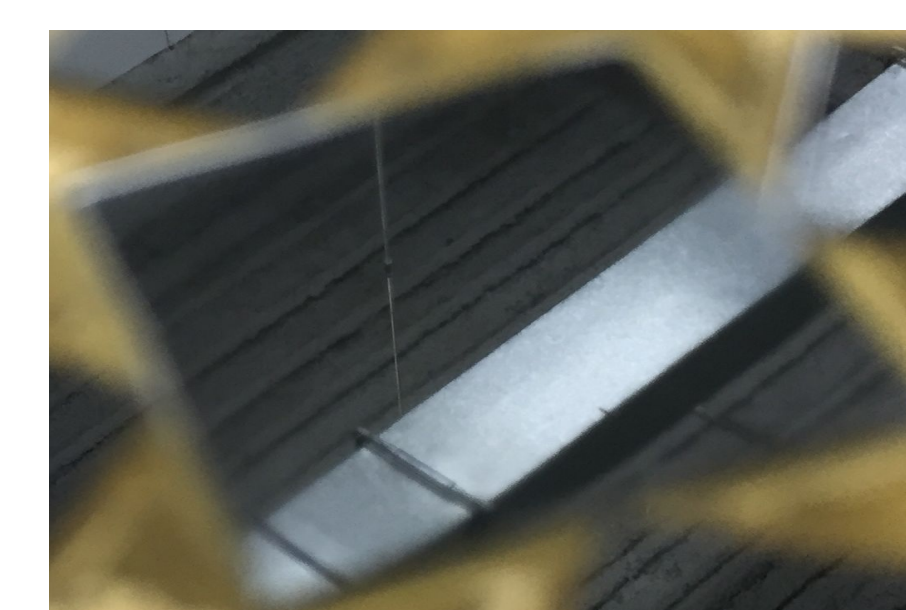
Before CMP  
Laser Microscope at 150x



After CMP  
Laser Microscope at 10x



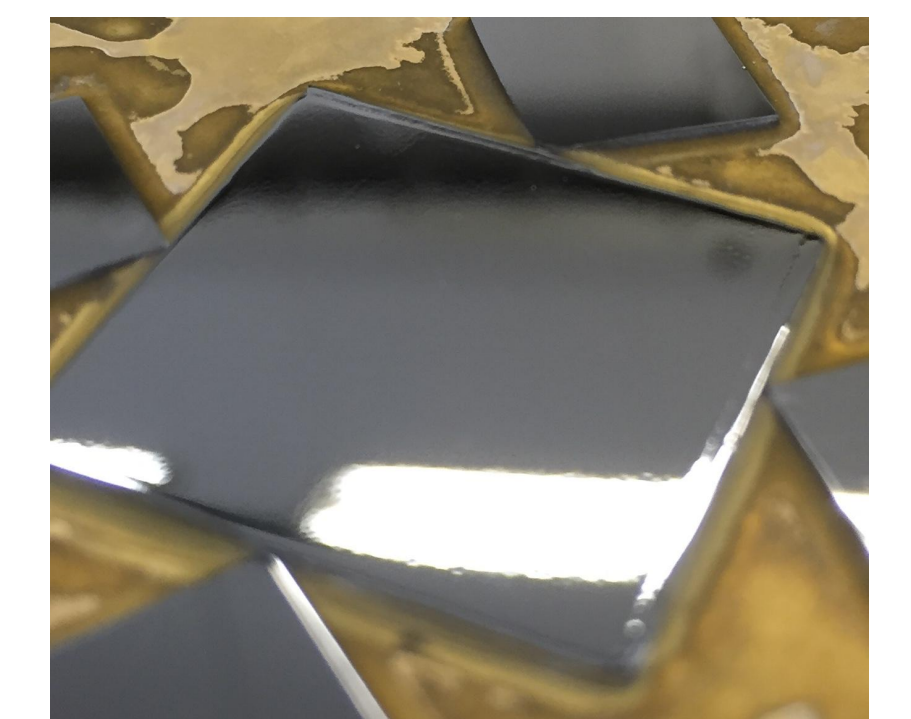
Camera View



AFM Rendering

## Discussion

- KOH used instead of  $\text{NH}_4\text{OH}$  in the polishing slurry
  - Si was etched anisotropically
  - Slight macroscopic roughness remained
  - Substrate edges were polished faster than the surface center
- Si used instead of SiGe to practice technique at low cost
- Limited available expertise on CMP



Remaining roughness and curved edges

### Conclusions

- Eliminated local surface roughness on Si
- Developed the foundations of CMP procedure for the laboratory

## Future Work

- Overhaul CMP machinery and improve experimental setup
- Characterize the polishing rate of SiGe under set pressure, velocity, and slurry conditions
- Finalize the procedure for CMP to be used in device fabrication

## References

- 1P. Shor, SIAM Journal of Computing **26**, 1484-1509 (1997).
- 2W. L. Chang, Emerging Research in Artificial Intelligence and Computational Intelligence: Int. Conf. Proc. **237**, 483-490 (2011).
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- 7H. Seidel, et al., J. Electrochem. Soc. **137**, 3612-3632 (1990).

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